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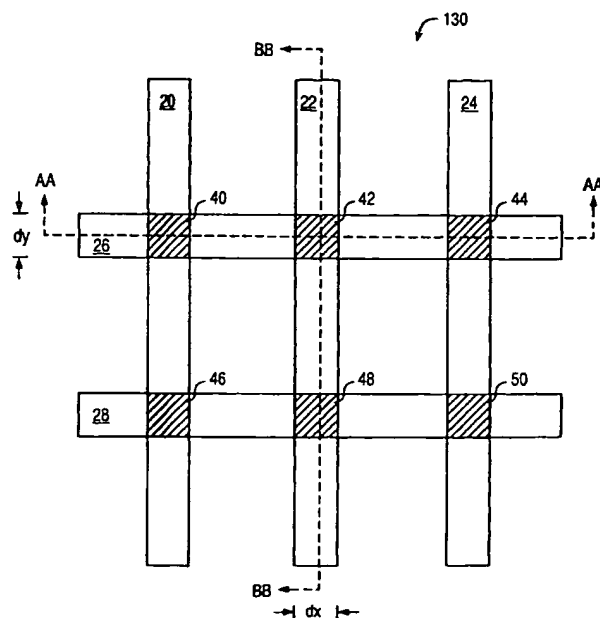
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(54) Magnetic memory

(57) A solid-state memory (130) including an array of magnetic storage cells (40-50) and a set of conductors (20-28). The process steps that pattern the conduc-

tors (20-28) also patterns the magnetic layers (40-50) in the magnetic storage cells (130) thereby avoiding the need to employ precise alignment between patterns masks.

FIG. 1



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Description

[0001] The present invention pertains to the field of solid-state memories. More particularly, this invention relates to a solid-state memory with magnetic storage cells.

[0002] Solid-state memories have a wide variety of applications particularly in computer systems. Prior solid-state memories are usually constructed of semiconductor materials. For example, prior semiconductor memories include dynamic random access memories (DRAMs) as well as persistent or nonvolatile memories such as flash memories to name a few.

[0003] A prior solid-state memory is typically arranged as one or more arrays of memory cells or storage cells. The structure of each storage cell usually provides a mechanism for storing a bit of information. For example, the storage cells in a typical DRAM include structures that form a capacitor for storing information as an electrical charge. In addition, the storage cells in a typical flash memory include structures that form a floating-gate for persistent storage of an electrical charge.

[0004] Typically, such specialized structures in prior solid-state memories require critical alignment in order to achieve high storage cell densities. For example, high density DRAM cells usually require critical alignments in the trenched or stacked capacitor structures contained therein. In addition, flash cells typically require critical alignment among the floating-gate structures contained therein.

[0005] Such storage cell structures are usually formed using multiple pattern masks according to the particular process technology used for fabrication of the solid-state memory. Typically, the critical alignments of such structures requires a relatively precise alignment among the pattern masks.

Unfortunately, process technologies that achieve precise alignment of pattern masks are usually expensive and therefore greatly increase the cost of prior high density solid-state memories.

[0006] In addition, prior solid-state memories usually are formed on single crystalline semiconductor materials. Unfortunately, the requirement of a crystalline semiconductor substrate limits the flexibility in which any storage cells may be arranged. For example, a typical crystalline semiconductor substrate used for fabricating prior solid-state storage cells usually precludes the stacking of arrays of DRAM or flash storage cells into multiple layers. Such limitations limit the storage densities that may be achieved with prior solid-state memories.

[0007] The preferred embodiment seeks to provide an improved memory.

[0008] According to an aspect of the present invention there is provided a memory as specified in claim 1.

[0009] The preferred embodiment provides a solid-state memory which includes an array of magnetic storage cells and a set of conductors coupled to the mag-

netic storage cells. The solid-state memory is manufactured so that the process steps that pattern the conductors also pattern the magnetic layers in the magnetic storage cells, thereby avoiding the need to employ precise alignment between pattern masks. In addition, the magnetic storage cells are not formed on a single crystalline semiconductor substrate. As a consequence, the arrangement of magnetic storage cells is not limited by the inherent limitations of such substrates.

[0010] An embodiment of the present invention is described below, by way of example only, with reference to the accompanying drawings, in which:

Figure 1 is a top view of a solid-state memory which includes an array of magnetic storage cells and an array of conductors that enable read and write access to the magnetic storage cells;

Figures 2a-2b illustrates the storage of a data bit in a magnetic storage cell;

Figure 3a is a cross-sectional view AA which shows a series of materials which are initially deposited onto a substrate and which are subsequently formed into conductors and magnetic storage cells;

Figure 3b is a cross-sectional view AA which illustrates patterning of the material shown in Figure 3a;

Figure 3c is a cross-sectional view AA which shows a thin layer of protective dielectric that covers the sides of the patterned stacked structures and the exposed area of the substrate;

Figure 3d is a cross-sectional view BB which shows a conductor material and top conductor photoresist deposited over the stacked structures and the protective dielectric;

Figure 3e is a cross-sectional view BB which shows the results of a milling step which stops before the strip of pinned magnetic film;

Figure 4 shows an arrangement for reading a magnetic storage cell;

Figure 5 shows an alternative arrangement of a magnetic storage cell which incorporates a diode structure to increase the signal to noise ratio during read operations.

[0011] Figure 1 is a top view of a solid-state memory 130 which includes an array of magnetic storage cells 40-50. The solid-state memory 130 also includes an array of conductors 20-28 that enable read and write access to the magnetic storage cells 40-50. The magnetic storage cells 40-50 use magnetic fields to store information. Each of the magnetic storage cells 40-50 ena-

bles storage of a corresponding bit of information which may be referred to as a data bit.

[0012] The magnetic storage cells 40-50 and the conductors 20-28 are formed onto a substrate 10. The conductors 20-28 are arranged as a set of top conductors 26-28 and an orthogonal set of bottom conductors 20-24. Each of the magnetic storage cells 40-50 has rectangular dimensions d_x and d_y which are defined by the widths of the bottom conductors 20-24 and the widths of the top conductors 26-28, respectively.

[0013] Figures 2a-2b illustrates the storage of a data bit in the magnetic storage cell 42. The magnetic storage cell 42 includes a magnetic film 60 and a magnetic film 64 which are separated by a dielectric region 62. The structure and the functionality of the remaining storage cells 40-50 are substantially similar to that of the magnetic storage cell 42. The orientation of magnetization in the magnetic film 60 is shown as M1 and the orientation of magnetization in the magnetic film 64 is shown as M2.

[0014] One of the magnetic films 60 and 64 has a fixed orientation of magnetization while the other has a non-fixed orientation of magnetization. The one of the magnetic films 60 and 64 having a non-fixed orientation of magnetization is the active magnetic film of the magnetic storage cell 42. The active magnetic film rotates its orientation of magnetization in response to electrical signals applied to the conductors 22 and 26 during write operations to the magnetic storage cell 42. In one embodiment, a first logic state of the data bit stored in the magnetic storage cell 42 is indicated when M1 and M2 are parallel and a second logic state is indicated when M1 and M2 are anti-parallel.

[0015] In other embodiments, other arrangements of magnetic orientations may be employed for storing information in the magnetic storage cell 42. For example, the pinned magnetic film in the magnetic storage cell may be switched and in response the non-pinned magnetic film switches to be anti-parallel to the pinned magnetic film. The pinned magnetic film may be the top magnetic film 60 or the bottom magnetic film 64.

[0016] In one embodiment, the magnetic film 64 is pinned with a fixed orientation of magnetization M2 while the magnetic film 60 has non-fixed orientation of magnetization M1. The orientation of magnetization M1 in the magnetic film 60 changes in response to electrical signals applied to the conductors 22 and 26 during write operations to the magnetic storage cell 42.

[0017] Figure 2a illustrates a "0" logic state of a data bit stored in the magnetic storage cell 42. In the "0" logic state the orientation of magnetization in the magnetic film 60 (M1) is antiparallel to the orientation of magnetization M2 in the magnetic film 64. Figure 2b shows a "1" logic state of the magnetic storage cell 42. In the "1" logic state, M1 is parallel to M2.

[0018] The magnetic storage cell 42 is read by applying a voltage potential, which may be referred to as a read voltage, across the conductors 26 and 22. The read

voltage causes an electrical current, also known as a sense current, to flow between the magnetic films 60-64 as electrical charge migrates through the dielectric region 62 according to a phenomenon known as spin tunneling. The storage cell 42 may be referred to as a spin tunneling storage cell.

[0019] The resistance of the magnetic storage cell 42 differs according to the orientations of M1 and M2. When M1 and M2 are antiparallel, the "0" logic state, the resistance of the magnetic storage cell 42 is at its highest. On the other hand, the resistance of the magnetic storage cell 42 is at its lowest when M1 and M2 are parallel which corresponds to the "1" logic state. As a consequence, the logic state of the data bit stored in the magnetic storage cell 42 can be determined by measuring its resistance. The resistance of the magnetic storage cell 42 is reflected by the magnitude of the sense current that flows in response to the read voltage applied to the conductors 22 and 26.

[0020] Figures 3a-3e illustrate the formation of the array of magnetic storage cells 40-50 and the conductors 20-28 on the substrate 10. In one embodiment, the substrate 10 is a silicon substrate that accommodates the formation of support electronics or the solid-state memory 130 such as sense amplifier and multiplexor circuitry. The process steps for the formation of the magnetic storage cells 40-50 and the conductors 20-28 does not require that the substrate 10 be a semiconductor material.

[0021] Figure 3a is a cross-sectional view AA which shows a series of materials 70-78 which are initially deposited onto the substrate 10. A layer of conductor material 70 is deposited onto the substrate 10 and provides a layer of conductive material for the formation of the conductors 20-24 which are the bottom conductors for the solid-state memory 130. The conductor material 70 is a sheet of conductive material such as copper, aluminum, or gold, or alloys of these materials.

[0022] In one embodiment, an antiferromagnetic material 72 is deposited on top of the conductor material 70. The antiferromagnetic material 72 provides a magnetic pinning material for fixing the orientations M2 in the magnetic storage cells 40-50 to be formed on the substrate 10. The antiferromagnetic material 72 may be iron-manganese (FeMn) or nickel-manganese (NiMn). Alternative materials for the antiferromagnetic material 72 include NiO and IrMn.

[0023] A magnetic film 74 is deposited on top of the antiferromagnetic material 72. The effect of magnetic exchange coupling between the magnetic film 74 and the antiferromagnetic material 72 pins the orientation of the magnetization in the magnetic film 74. The magnetic film 74 provides a layer of pinned magnetic material for forming the pinned magnetic film regions of the magnetic storage cells 40-50. For example, the magnetic film 74 is subsequently formed into the pinned magnetic film 64 of the magnetic storage cell 42. The magnetic film 74 may be nickel-iron (NiFe) or cobalt or alloys or layers

comprised of combinations of these materials. Alternative materials for the magnetic film 74 include Fe_3O_4 and CrO_2 or other ferromagnetic or ferrimagnetic materials.

[0024] An insulating material 76 is deposited on the magnetic film 74. The insulating material 76 provides a layer for forming the dielectric regions of the magnetic storage cells 40-50, such as the dielectric region 62 of the magnetic storage cell 42. In one embodiment, the insulating material 76 is aluminum-oxide (Al_2O_3). Alternative materials of the insulating material 76 include silicon-dioxide (SiO_2), tantalum-oxide (Ta_2O_5), and silicon-nitride (Si_3N_4).

[0025] A magnetic film 78 is deposited on top of the insulating material 76. The magnetic film 78 provides a layer of material for forming the active regions of the magnetic storage cells 40-50, such as the magnetic film 60 of the storage cell 42. The magnetic film 78 may be nickel-iron (NiFe) or cobalt or alloys or layers comprised of combinations of these materials. Alternative materials for the magnetic film 78 include Fe_3O_4 and CrO_2 or other ferromagnetic or ferrimagnetic materials.

[0026] Figure 3b is a cross-sectional view AA which illustrates a patterning of the material shown in Figure 3a. The patterning is performed by forming lines of photo-resist, including the photo-resist 80, on top of the magnetic film 78 using photolithography. The line of photo-resist 80 defines the length of the bottom conductor 22 and the d_x dimension of the bottom conductor 22 and the magnetic storage cells 42 and 48. An ion milling operation is performed to remove the materials from the substrate 10 that are not protected by photoresist. The ion milling operation may be performed, for example, with a bombardment of argon ions. The protection provided by the photo-resist 80, for example, results in the formation of a stacked structure 82 from the materials shown in Figure 3a.

[0027] The stacked structure 82 includes the bottom conductor 22 which is a remnant of the conductor material 70. The stacked structure 82 also includes a strip of antiferromagnetic material 90 which remains from the antiferromagnetic material 72. The strip of antiferromagnetic material 90 pins the magnetic orientations M2 of the magnetic storage cells 42 and 48 in a direction parallel to the length of the conductor 22.

[0028] The stacked structure 82 includes a strip of magnetic film 92, a strip of dielectric material 94, and a strip of magnetic film 96, which remain from the magnetic film 74, the dielectric material 76, and the magnetic film 78, respectively. The strips of magnetic film 92, dielectric material 94, and the magnetic film 96 are to be formed into the magnetic storage cells 42 and 48 with subsequent patterning steps.

[0029] Figure 3c is a cross-sectional view AA which shows a thin layer of protective dielectric 100 that covers the sides of the stacked structure 82 and the exposed area of the substrate 10. The protective dielectric 100 is initially deposited over the stacked structure 82, and the photo-resist 80 and exposed areas of the substrate 10

as a thin layer, for example 500Å or less, of dielectric material. The photo-resist 80 and other lines of photo-resist used for patterning the conductors 20-24 are then removed using for example an ultrasonic agitator with a solvent. The resulting protective dielectric 100 prevents short circuits between edges of the magnetic films 92 and 96 after the conductors 26 and 28 are formed.

[0030] Figure 3d is a cross-sectional view BB which shows a conductor material 102 deposited over the stacked structure 82 and the protective dielectric 100. The conductor material 102 provides a layer of conductive material for the formation of the top conductors 26-28. The conductor material 102 is a sheet of conductive material such as copper, aluminum, or gold, or alloys of these materials.

[0031] The top conductors 26-28 are then patterned from the conductor material 102. The patterning of the top conductors 26-28 forms the d_y dimensions of the magnetic storage cells 40-50 and the top conductors 26-28 and automatically aligns the top conductors 26-28 and the layers of the magnetic storage cells 40-50. The top conductors 26-28 are patterned by forming lines of photo-resist including the lines of photo-resist 110-112 on top of the conductor material 102 using photolithography. The lines of photo-resist 110-112 each have a width d_y .

[0032] An ion milling step is used to remove materials not protected by the photo-resist 110-112. In one embodiment, the milling step is used to remove materials down to the strip of antiferromagnetic material 90. In another embodiment, the milling step is stopped before the strip of magnetic film 92 is removed. The photo-resist 110-112 is then stripped away.

[0033] Figure 3e is a cross-sectional view BB which shows the results of the milling step which stops before the removal of the magnetic film 92. The magnetic storage cell 42 is shown with the magnetic film 60 and the dielectric region 62 formed from the strip of magnetic film 96 and the strip of dielectric material 94, respectively. The magnetic storage cell 48 includes a magnetic film 126 and a dielectric region 124 formed from the strip of magnetic film 96 and the strip of dielectric material 94, respectively.

[0034] The strip of magnetic material 92 provides a continuous pinned magnetic film for both the magnetic storage cells 42 and 48. This embodiment prevents magnetic fields that would otherwise emanate from patterned edges of the magnetic material 92 from affecting the magnetic fields in the active magnetic films of magnetic storage cells 42 and 48. The exchange coupling effect between the strip of magnetic material 92 and the magnetic films 62 and 124 pins the orientations of the magnetic flux in the magnetic films 62 and 124 in a direction that runs along the length of the strip of magnetic material 92 which is also parallel to the length of the bottom conductor 22.

[0035] The patterning of the top conductors 26 and 28 patterns and automatically aligns the active magnetic

films in the magnetic storage cells 42 and 48 to provide the aligned d_x and d_y dimensions. As a consequence, there is no need to use separate pattern masks for the conductors 26-28 and the active layers or dielectric layers of the magnetic storage cells 42 and 48 nor to precisely align any such pattern masks.

[0036] The structure shown in Figure 3e may subsequently be planarized, using for example an dielectric layer, and another array of magnetic storage cells formed on top of the magnetic storage cells 40-50. This is possible because no single crystalline semiconductor substrate is required. The ability to have many layers of magnetic storage cells enhances the overall density that can be attained in the solid-state memory 130.

[0037] Figure 4 shows an arrangement for reading the magnetic storage cell 42. The magnetic storage cell 42 is read by applying a read voltage V_{rd} to the conductor 26 and coupling the conductor 22 to an input 150 of a current sense amplifier 160. The potential V_{rd} across the magnetic storage cell 42 causes a sense current to flow into the input 150 of the current sense amplifier 160. The magnitude of the sense current indicates the resistance of the magnetic storage cell 42 and therefore its logic state.

[0038] During the read operation, the conductors 20 and 24 are applied with a ground potential using a pair of transistors 200-202. In addition, the input 150 of the current sense amplifier 160 has a virtual ground potential which means that the conductor 22 has a virtual ground potential. The ground and virtual ground potentials of the conductors 20-24 reduce the amount of current flow between the conductors 20-24. This current flow is known as leakage current. The reduced amount of leakage current in the conductors 20-24 increases the signal to noise ratio during read operations on the magnetic storage cell 42.

[0039] The equalized potentials among the conductors 20-24 can be accomplished using a variety of circuits. For example, the transistors 200-202 may apply a potential V_x to the conductors 20 and 24 and the input 150 may have a potential of V_x . In addition, each of the conductors may be coupled to an input of a corresponding current sense amplifier. The inputs of the current sense amplifiers may be virtual grounds or may have some other potential so long as the potentials of all the conductors 20-24 are equalized. Moreover, any combination of transistors and current sense amplifiers may be used to equalize the potentials of the conductors 20-24 during read operations.

[0040] Figure 5 shows an alternative arrangement of the magnetic storage cells 40-50 which incorporates a diode structure to increase the signal to noise ratio during read operations. For example, the magnetic storage cell 42 in this arrangement includes a diode structure formed from a platinum layer 180 and a silicon layer 182. A high temperature processing step is used to form polysilicon from the silicon layer 182 prior to the deposition of the materials 60-64.

[0041] The conductors 20-28 have a relatively low impedance compared to the impedance of the spin tunneling junctions of the magnetic storage cells 40-50. However, as the size of the array of storage cells of the solid-state memory 130 increases, the loading effect of the conductors for the larger array can cause excessive leakage. Diode structures such as the one shown incorporated into the magnetic storage cells can decrease cross-talk or leakage current among the conductors. The decrease in leakage current increases the signal to noise ratio attainable during read operations particularly for large array sizes.

[0042] The disclosures in United States patent application no. 08/974,925, from which this application claims priority, and in the abstract accompanying this application are incorporated herein by reference.

Claims

1. A memory, comprising:

array of magnetic storage cells each for storing a bit of information;
a set of top conductors coupled to the magnetic storage cells formed in the same patterning step as the magnetic storage cells.

2. A memory as in claim 1, including:

a top magnetic film in each of the magnetic storage cells;
a top magnetic film and a dielectric region in each of the magnetic storage cells; or
a top magnetic film and dielectric region and a bottom magnetic film in each of the magnetic storage cells, formed in the same patterning step as the magnetic storage cells.

3. A memory as in claim 1, comprising a set of bottom conductors substantially orthogonal to the top conductors and coupled to the magnetic storage cells, wherein a patterning step that formed the bottom conductors also patterned a top magnetic film and a dielectric region and a bottom magnetic film in each of the magnetic storage cells.

4. A memory as in claim 1, comprising a dielectric layer operable to prevent the top conductors from causing short circuits among layers of the magnetic storage cells.

5. A memory as in claim 3, comprising:

a current sensing amplifier including an input coupled to one of the bottom conductors to sense an electrical current from one of the magnetic storage cells being read;

- circuitry for applying a potential to each of the bottom conductors not coupled to the magnetic storage cell being read such that the potentials of the bottom conductors not coupled to the magnetic storage cell being read are substantially equal to the potential of the input to the current sense amplifier to reduce an amount of leakage electrical current among the bottom conductors.
6. A memory as in claim 5, wherein the circuitry for applying a potential to each of the bottom conductors not coupled to the magnetic storage cell being read includes at least one transistor or at least one other current sense amplifier having an input with the potential.
7. A memory as in claim 1, wherein each magnetic storage cell includes a diode structure operable to reduce the amount of leakage electrical current during read operations in the memory.
8. A process of forming a memory having magnetic storage cells, comprising the steps of:
- depositing a bottom layer of conductor material onto a substrate;
 - depositing a set of layers of magnetic materials onto the bottom layer of conductor material;
 - patterning a set of bottom conductors from the bottom layer of conductor material such that the layers of magnetic materials are patterned into magnetic storage cells in the same step.
9. A process as in claim 8, comprising the step of depositing a dielectric layer over the layers of magnetic materials and the substrate.
10. A process as in claim 9, comprising the steps of:
- depositing a top layer of conductor material onto the dielectric layer;
 - patterning a set of top conductors from the top layer of conductor material such that the layers of magnetic materials are patterned in the same step.
11. A process as in claim 10, wherein the layers of magnetic materials include a top magnetic film and a bottom magnetic film and an intervening dielectric region.
12. A process as in claim 11, wherein the patterning step on the top conductors also patterns the top and the bottom magnetic films and the intervening dielectric region, or also patterns the top magnetic film and the intervening dielectric region but stops before patterning the bottom magnetic film.
13. A process as in claim 8, comprising the step of depositing a set of layers for forming a diode structure such that the patterning of the bottom conductors also patterns the layers for forming the diode structures.
14. A process as in claim 10, comprising the steps of:
- forming a planarized layer on the top conductors;
 - forming another layer of magnetic storage cells on top of the planarized layer.

FIG. 1

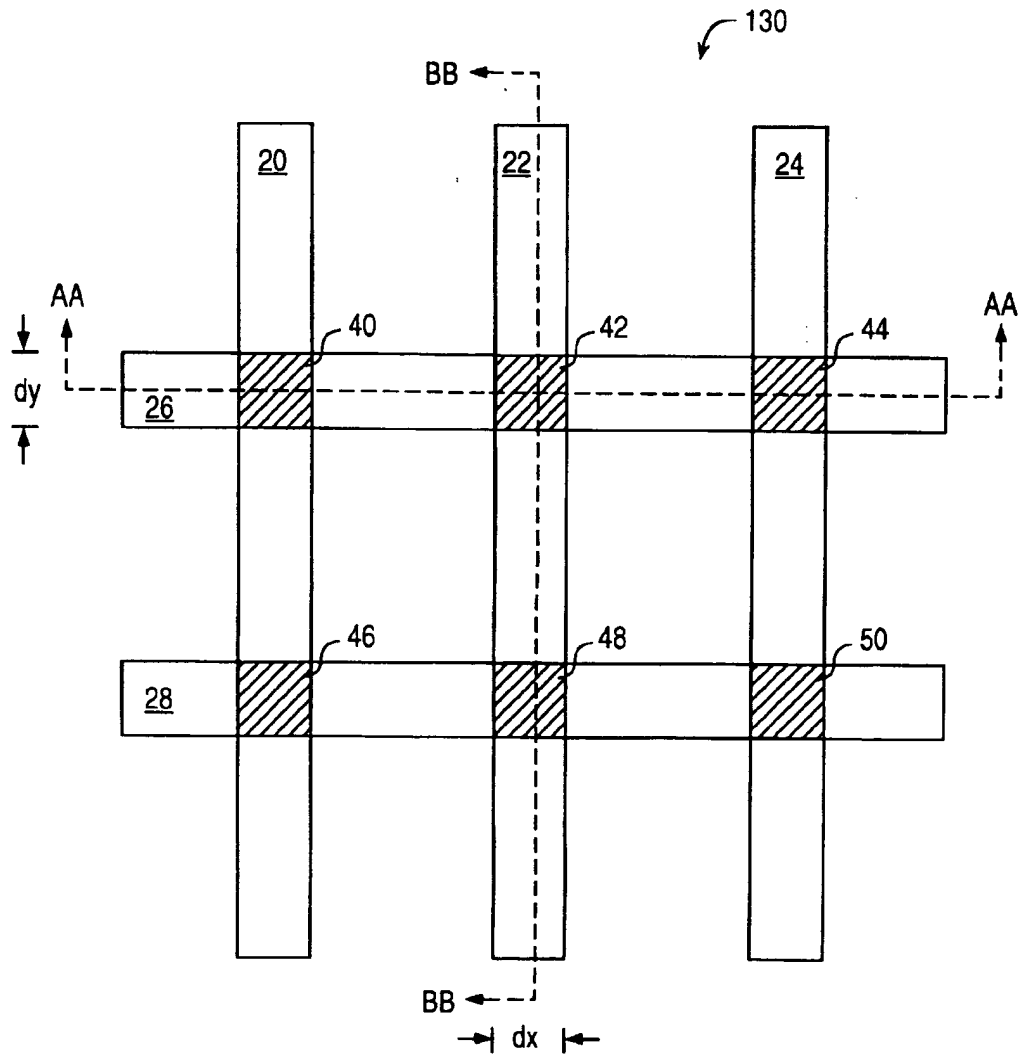


FIG. 2A

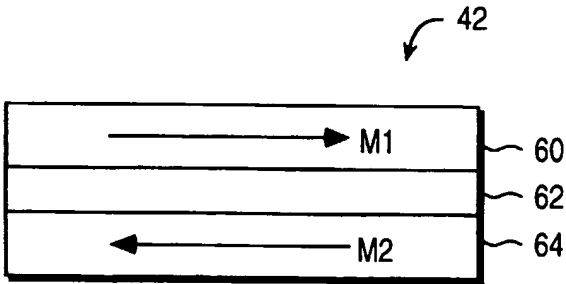


FIG. 2B

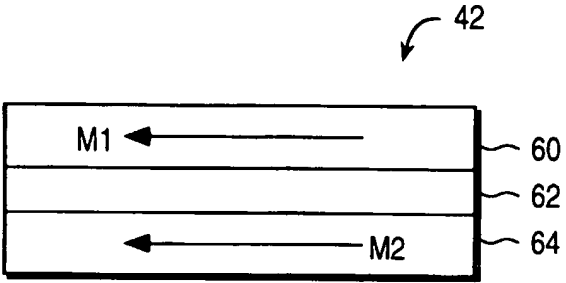


FIG. 3A

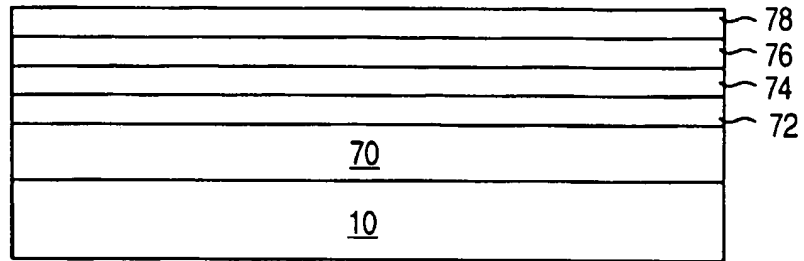


FIG. 3B

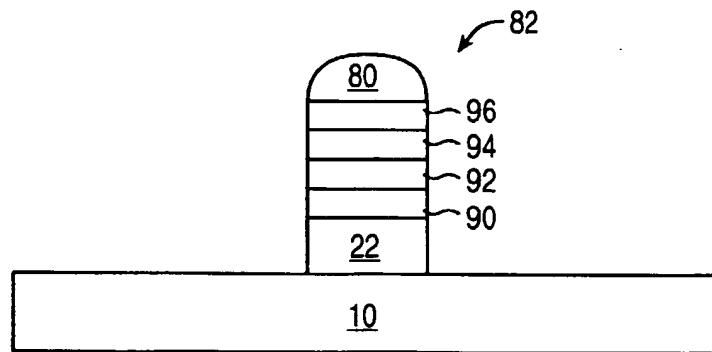
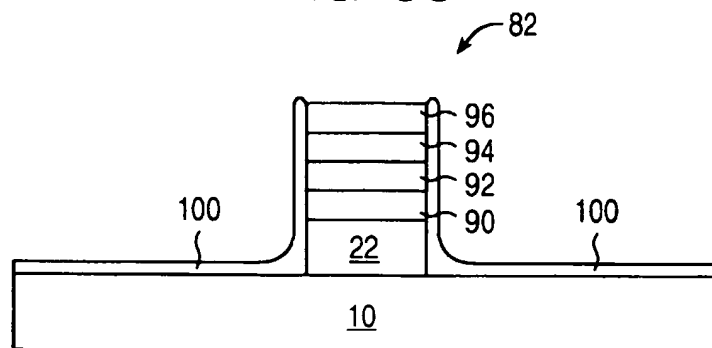


FIG. 3C



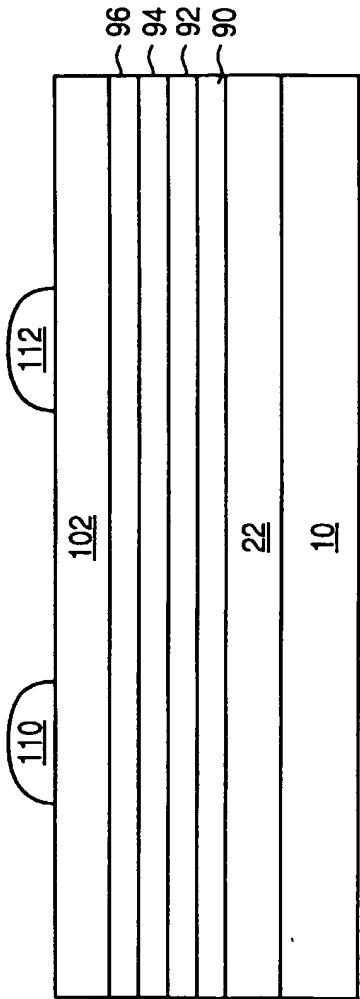


FIG. 3D

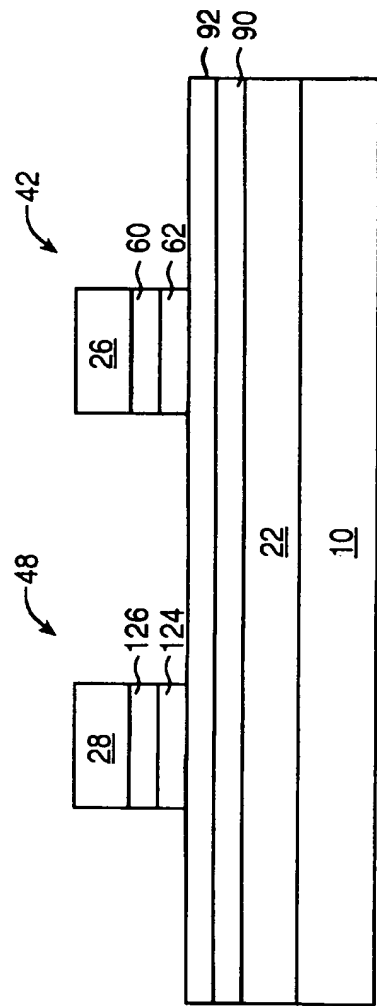


FIG. 3E

FIG. 4

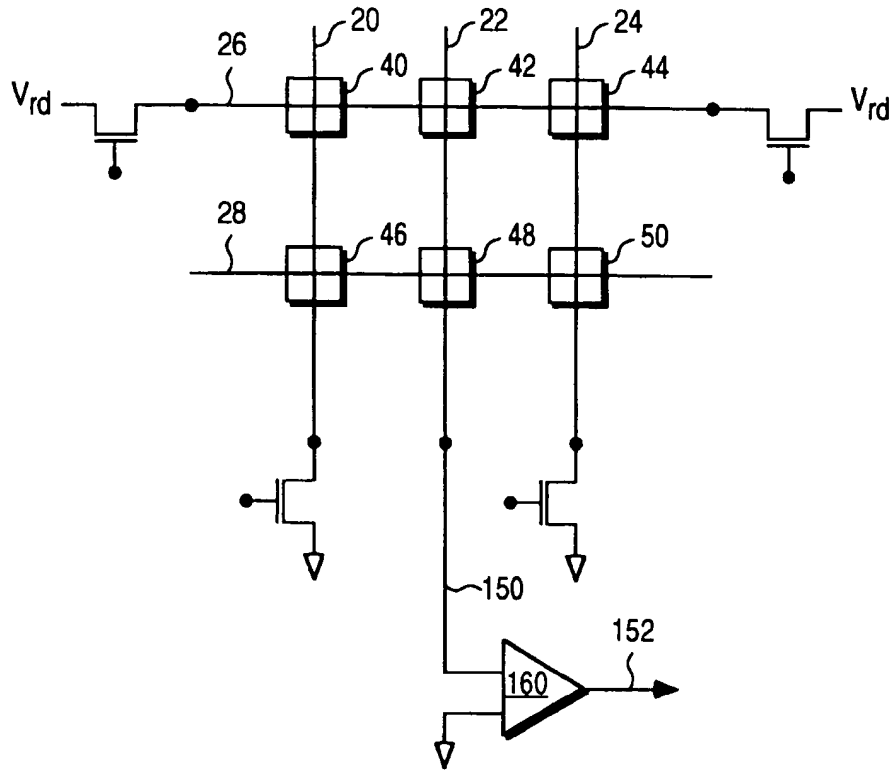


FIG. 5

